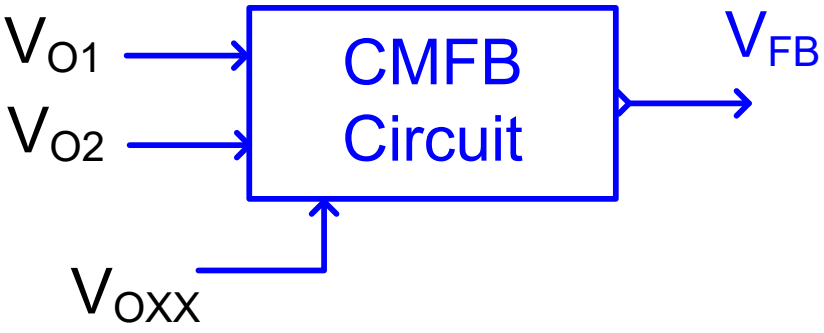
EE 435

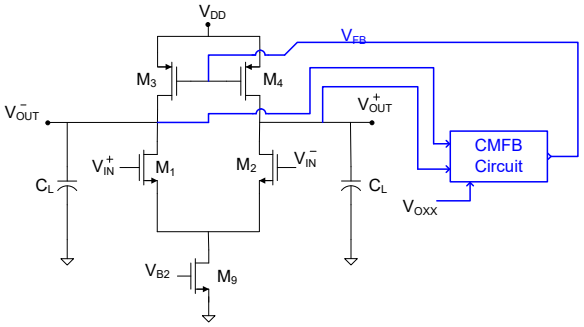
Lecture 24

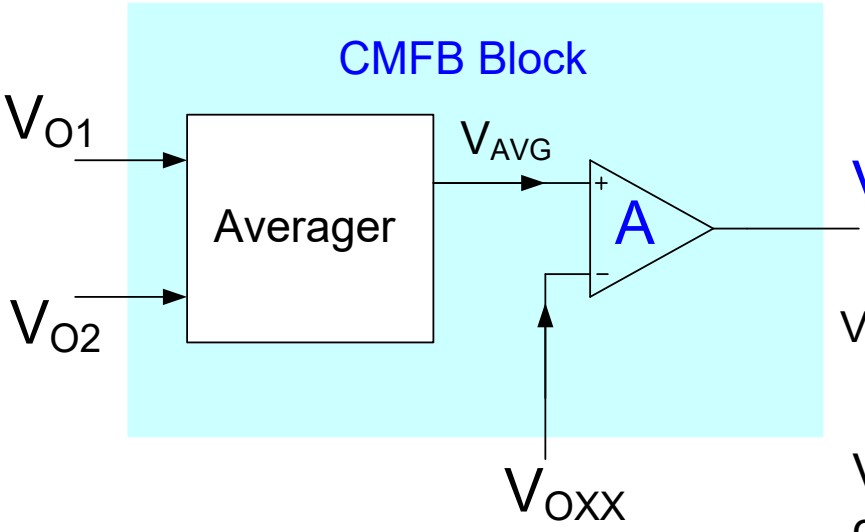
Data Converter Operation

Basic Operation of CMFB Block

Review from last lecture



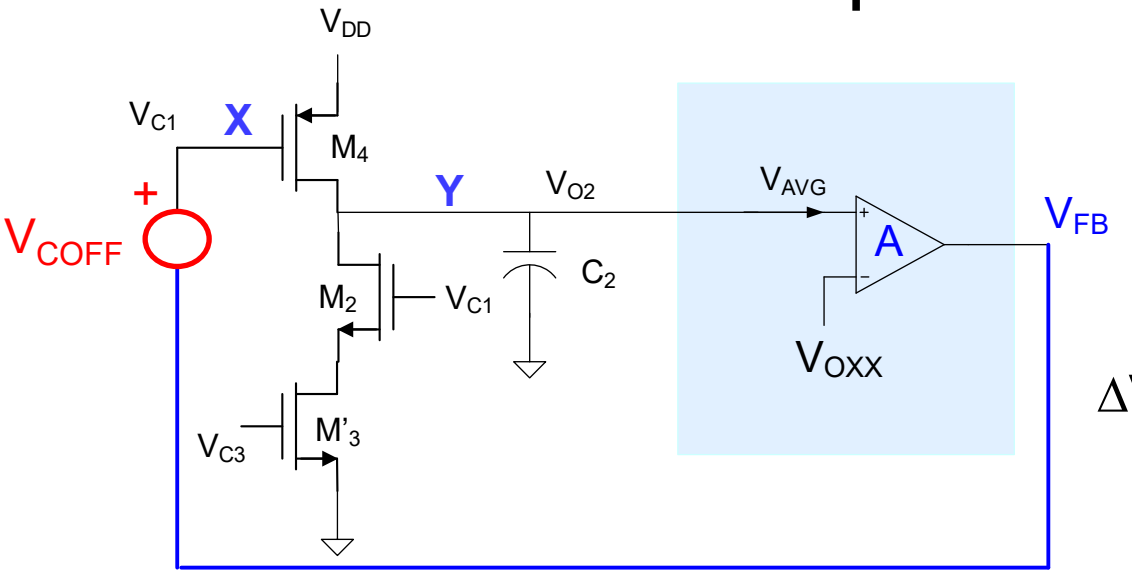


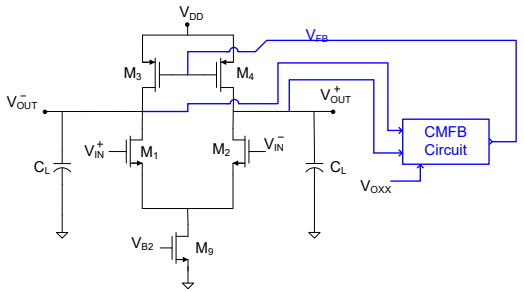


$$V_{FB}=\left(\frac{V_{01}+V_{02}}{2}\right)A(s)$$

V_{OXX} is the desired quiescent voltage at the stabilization node (irrespective of where V_{FB} goes)

How much gain is needed in the CMFB amplifier?





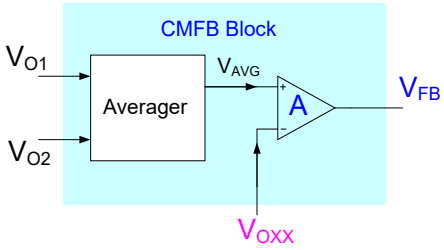
The CMFB Loop

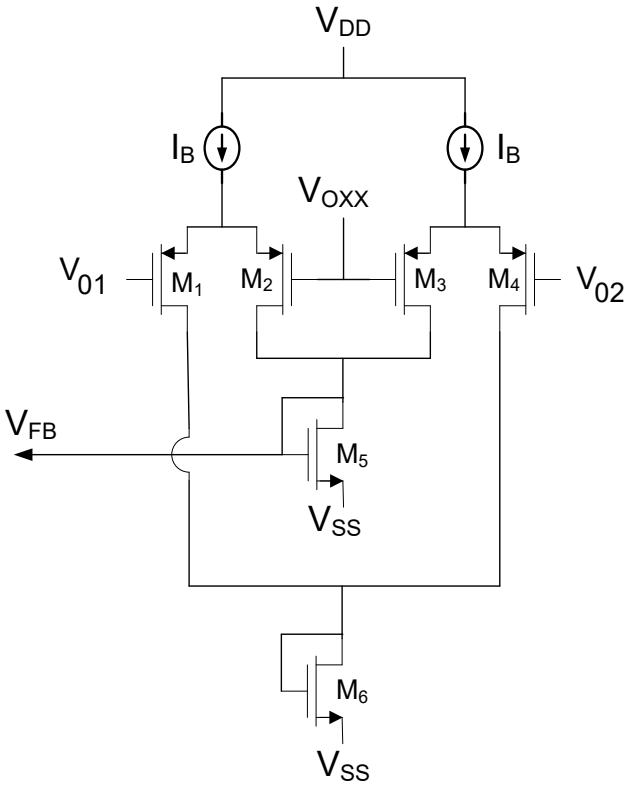
$$\Delta V_{0UT\text{-}ACCEPTABLE} = V_{COFF} \frac{A_{COM2}}{1 - AA_{COM2}}$$

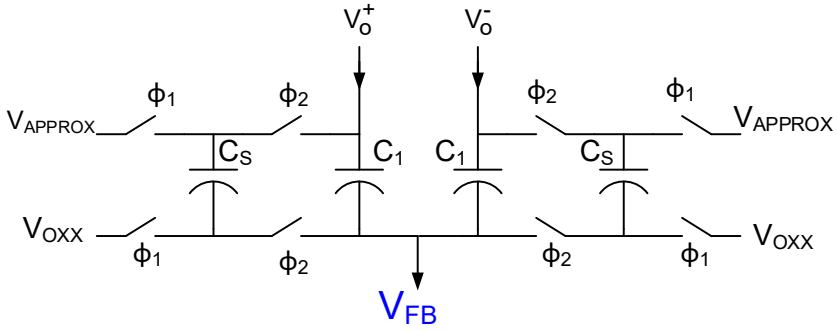
- This does not require a particularly large gain
- This is the loop that must be compensated since A and A_{COMP2} will be frequency dependent
- Miller compensation capacitor for compensation of differential loop will often appear in shunt with C_2
- Can create this “half-circuit” loop (without CM inputs on a fully differential structure) for simulations
- Results extend readily to two-stage structures with no big surprises
- Capacitances on nodes **X** and **Y** create poles for CMFB circuit
- Reasonably high closed-loop CMFB bandwidth needed to minimize shifts in output due to high-frequency common-mode noise

CMFB Circuits

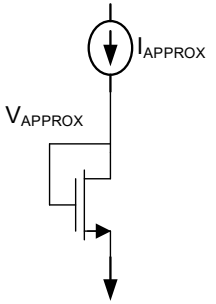
- Several (but not too many) CMFB blocks are widely used
- Can be classified as either continuous-time or discrete-time







C_S small compared to C_1



- V_{OXX} generated by simple bias generator
- φ_1 and φ_2 are complimentary non-overlapping clocks that run continuously

Data Converters

Types:

A/D (Analog to Digital)

Converts Analog Input to a Digital Output

D/A (Digital to Analog)

Converts a Digital Input to an Analog Output

A/D is the world's most widely used mixed-signal component

D/A is often included in a FB path of an A/D

A/D and D/A fields will remain hot indefinitely

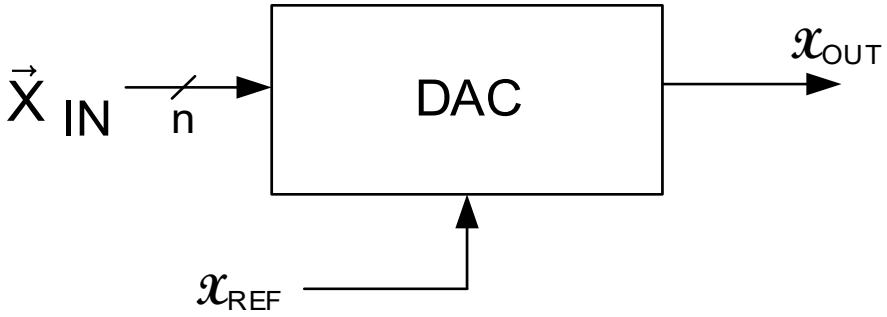
technology advances make data converter design more challenging

embedded applications

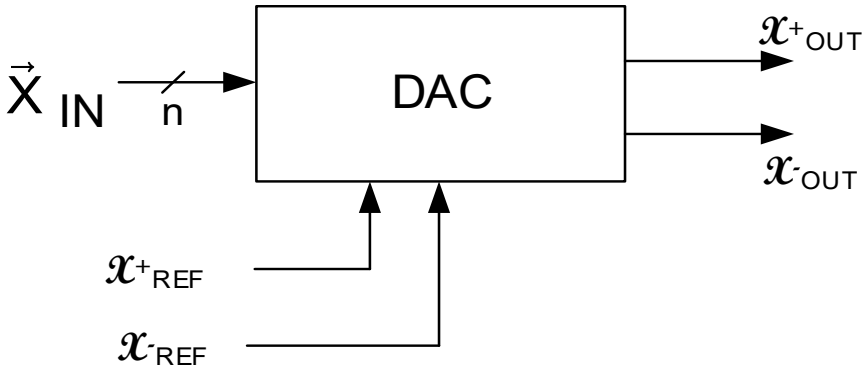
designs often very application dependent

D/A Converters

Basic structure:

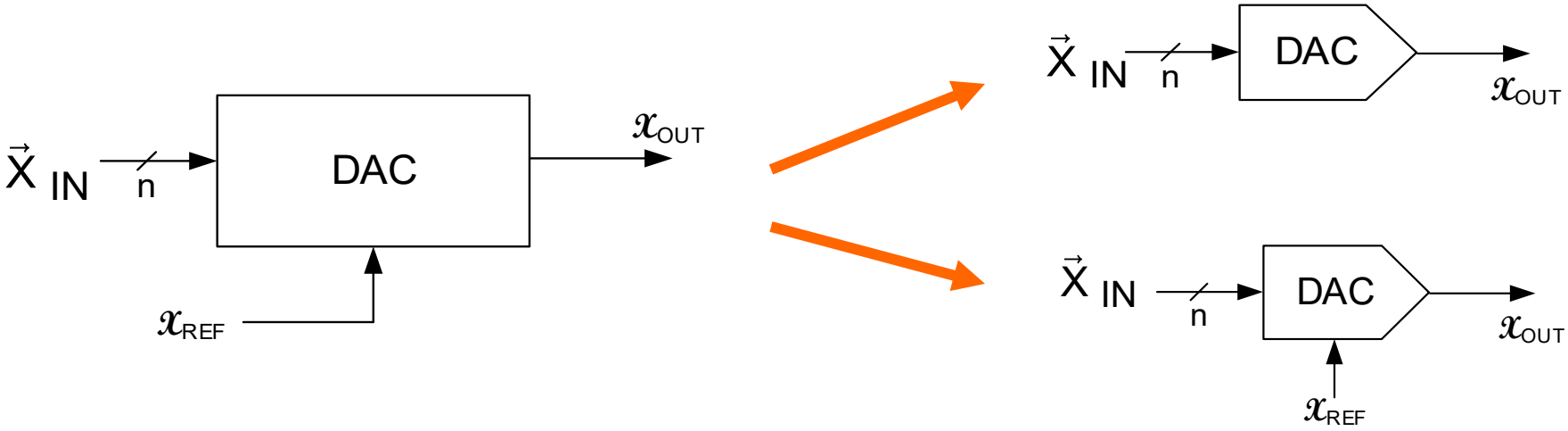


Basic structure with differential outputs::



D/A Converters

Notation:



x_{REF} is always present though often not shown on the symbol for the DAC

D/A Converters

$$\vec{X}_{IN}=<b_{n-1},b_{n-1},\ldots b_1,b_0>$$

b_0 is the Least Significant Bit (LSB)

b_{n-1} is the Most Significant Bit (MSB)

Number of ideal DAC outputs: $N=2^n$

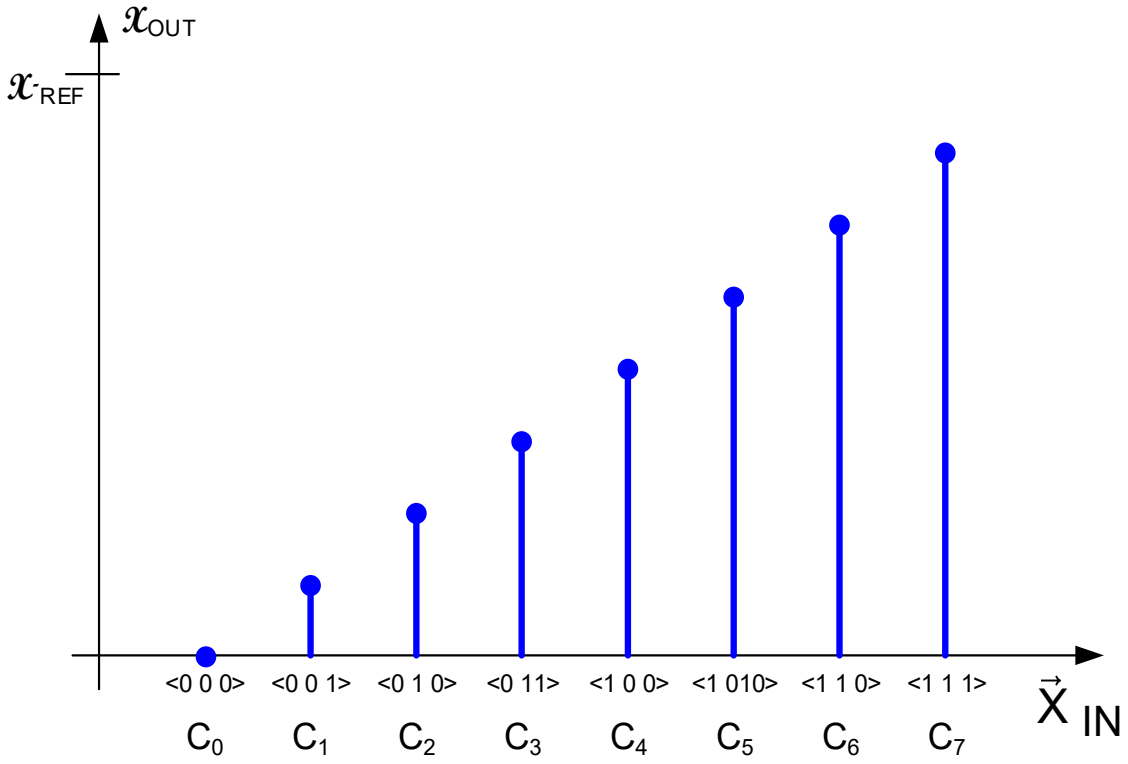
Note: some authors use different index notation

An Ideal DAC is characterized at low frequencies by its static performance

D/A Converters

$\vec{X}_{IN} = <b_{n-1}, b_{n-1}, \ldots b_1, b_0>$

An Ideal DAC transfer characteristic (3-bits)

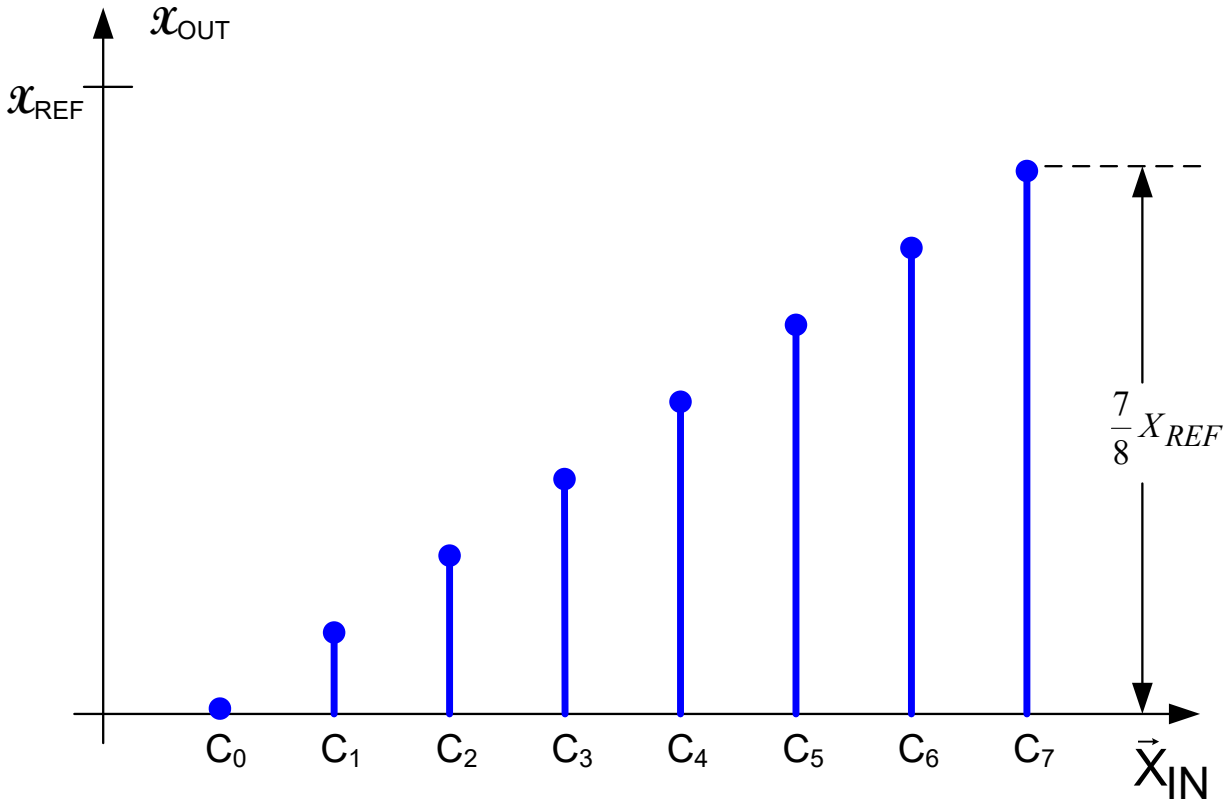


Code C_k is used to represent the decimal equivalent of the binary number $<b_{n-1} .. b_0)>$

D/A Converters

$\vec{X}_{IN}=<b_{n-1},b_{n-1},...b_1,b_0>$

An Ideal DAC transfer characteristic (3-bits)



D/A Converters

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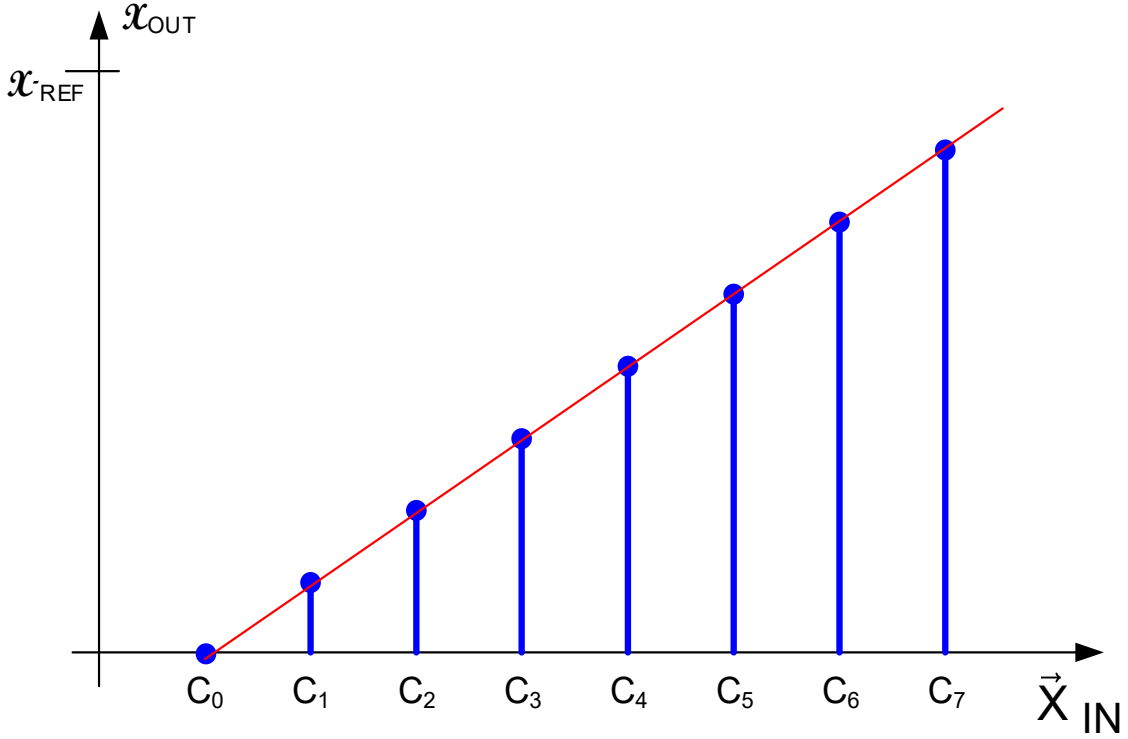
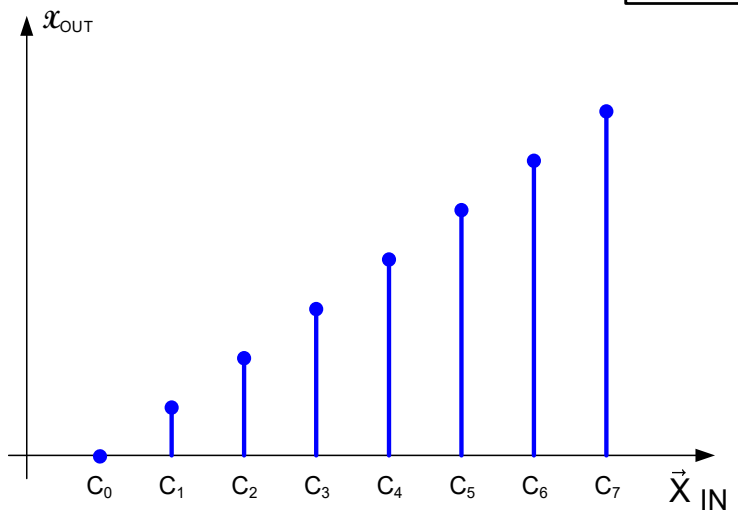


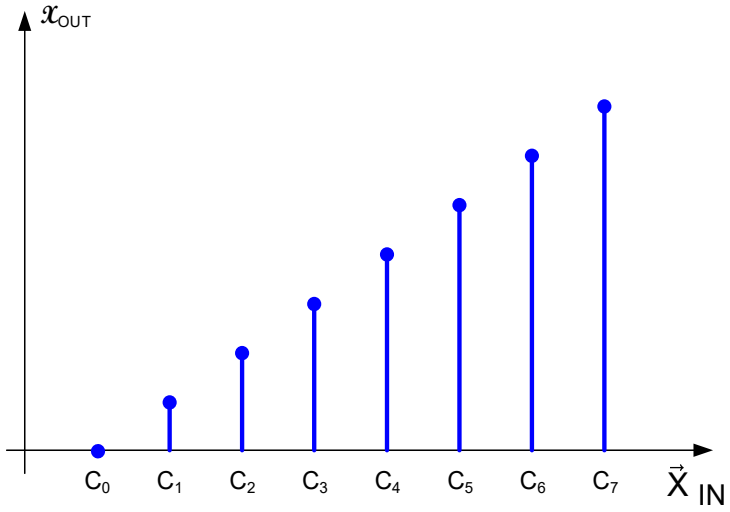
All points of this ideal DAC lie on a straight line

D/A Converters



- Most D/A ideally have a linear relationship between binary input and analog output
- Output represents a discrete set of continuous variables
- Typically this number is an integral power of 2, i.e. $N=2^n$
- $\vec{X}_{IN}$ is always dimensionless
- x_{OUT} could have many different dimensions
- An ideal nonlinear characteristic is also possible (waveform generation and companding)
- Will assume a linear transfer characteristic is desired unless specifically stated to the contrary

D/A Converters



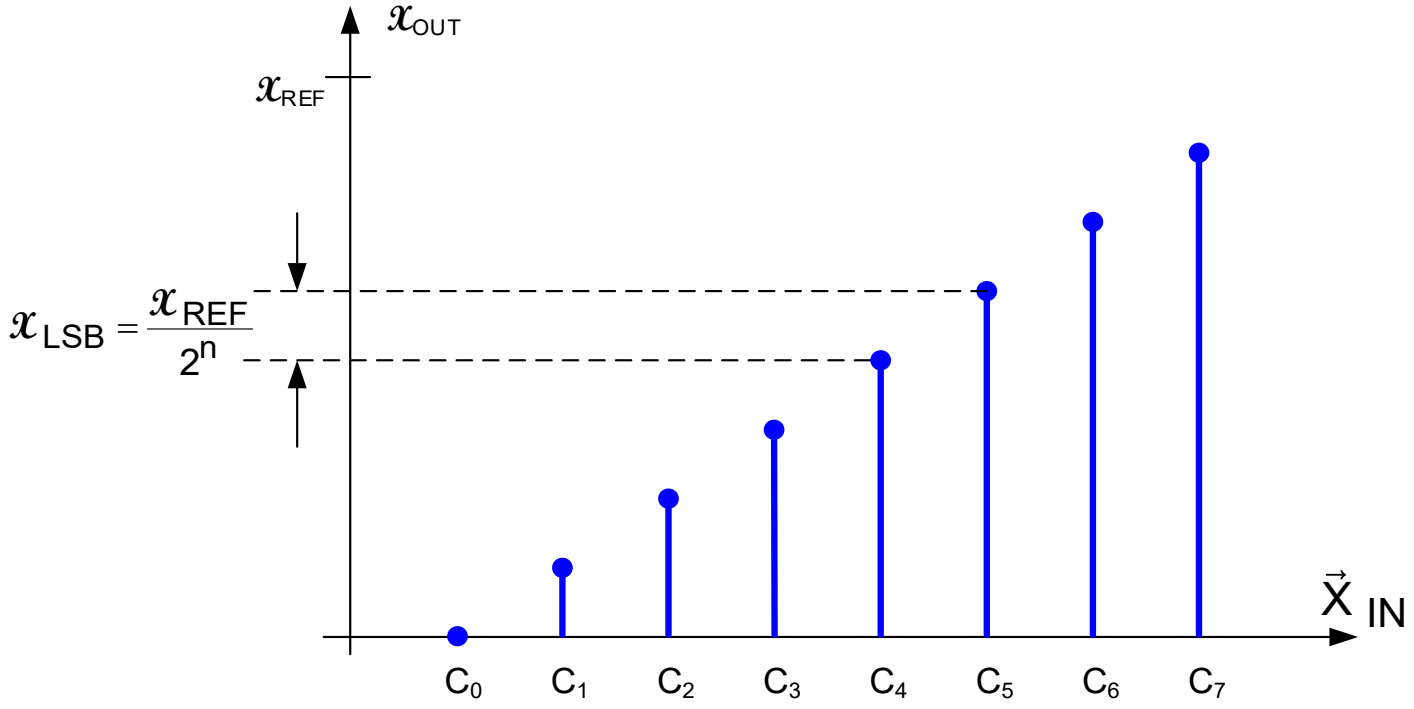
For this ideal DAC

$$x_{OUT} = X_{REF}\left(\frac{b_{n-1}}{2} + \frac{b_{n-2}}{4} + \frac{b_{n-3}}{8} + \ldots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}\right)$$

$$x_{OUT} = X_{REF}\sum_{j=1}^{n}\frac{b_{n-j}}{2^j}$$

- Number of outputs gets very large for n large
- Spacing between outputs is $X_{REF}/2^n$ and gets very small for n large

D/A Converters

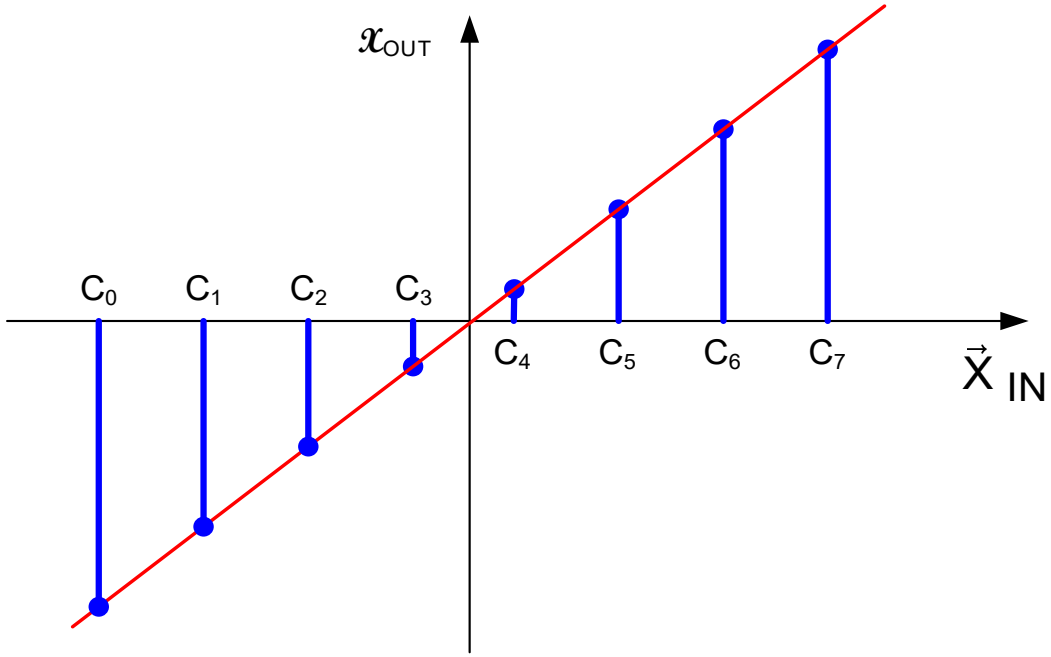


- Ideal steps all equal and termed the LSB
- x_{LSB} gets very small for small x_{REF} and large n

e.g. If x_{REF}=1V and n=16, then N=2^{16} =65,536, x_{LSB}=15.25μV

D/A Converters

An alternate ideal 3-bit DAC

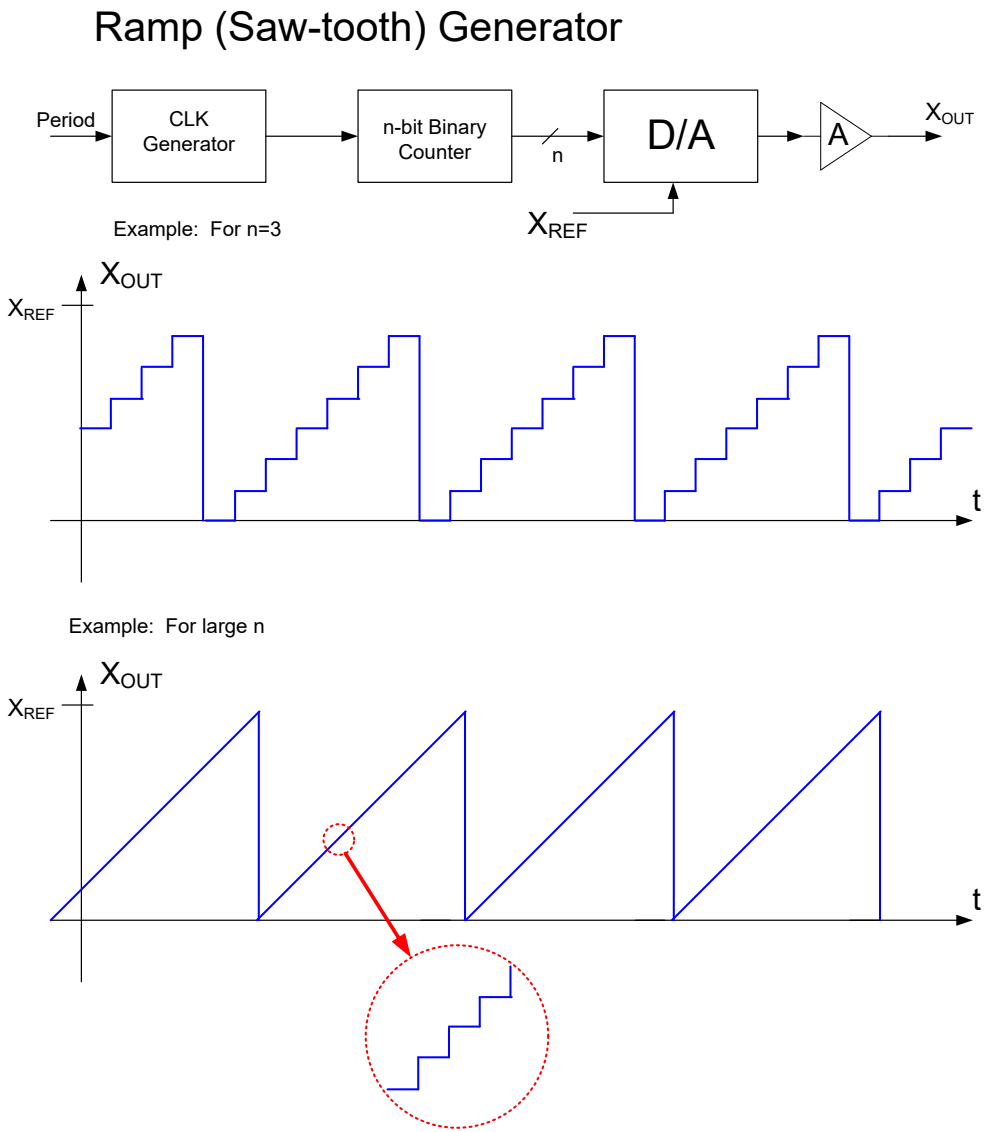


Irrespective of which form is considered, the increment in the output for one Boolean bit change in the input is x_{LSB} and the total range is 1LSB less than x_{REF}

Applications of DACs

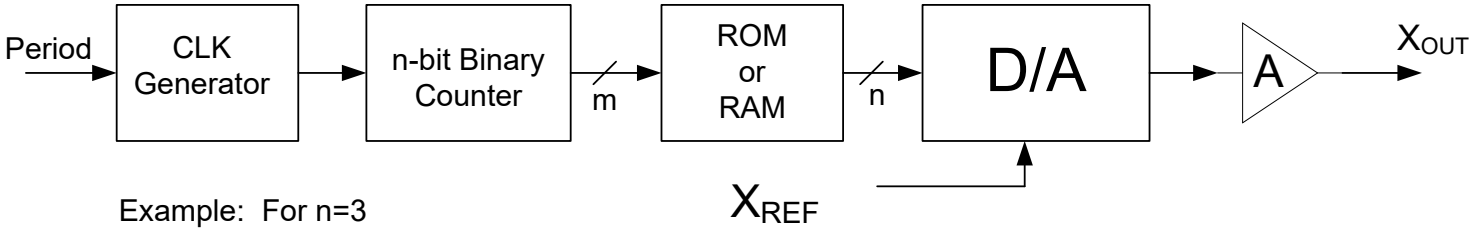
- Waveform Generation
- Voltage Generation
- Analog Trim or Calibration
- Industrial Control Systems
- Feedback Element in ADCs
- ….

Waveform Generation with DACs

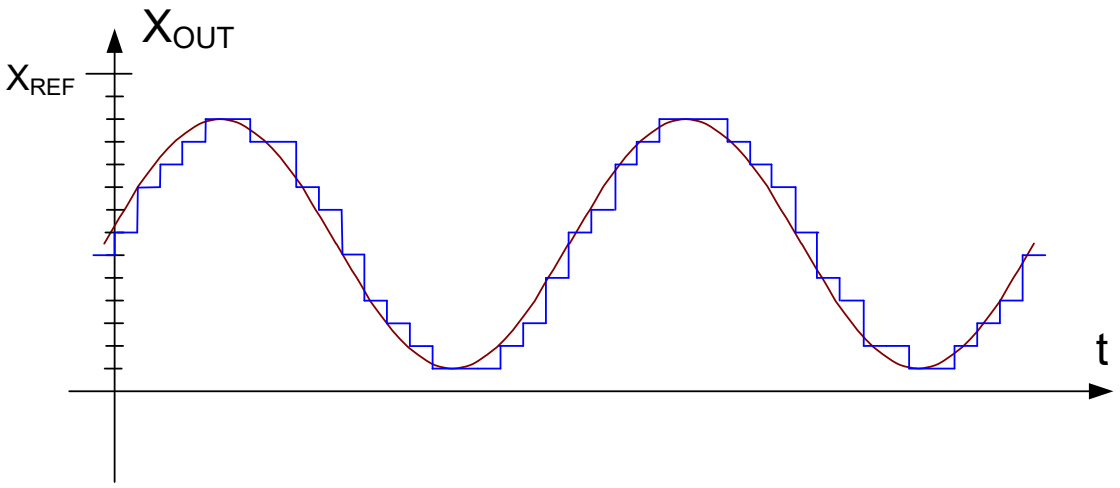


Waveform Generation with DACs

Sine Wave Generator



Example: For n=3

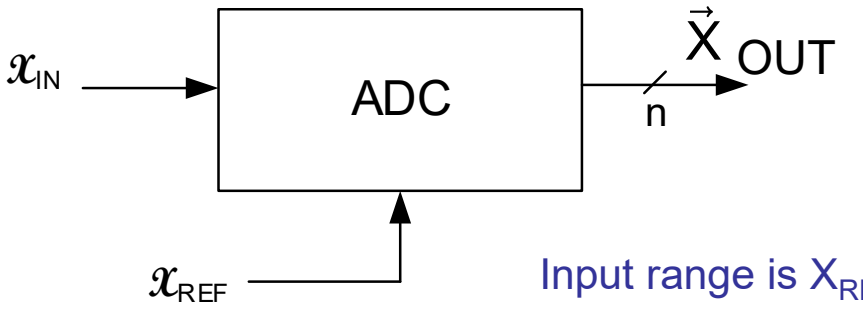


Distortion of the desired waveforms occurs due to both time and amplitude quantization

Often a filter precedes or follows the buffer amplifier to smooth the output waveform

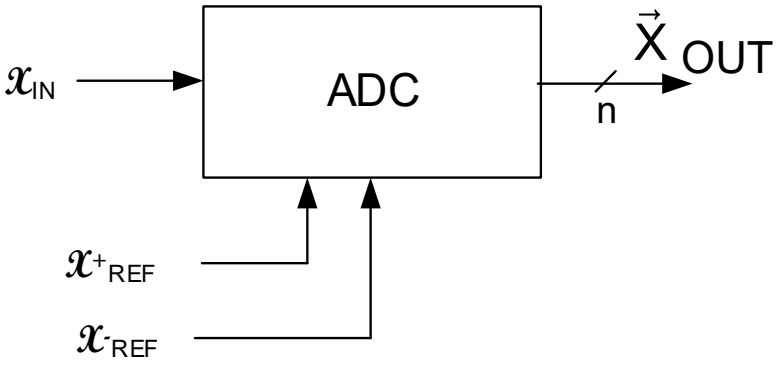
A/D Converters

Basic structure:

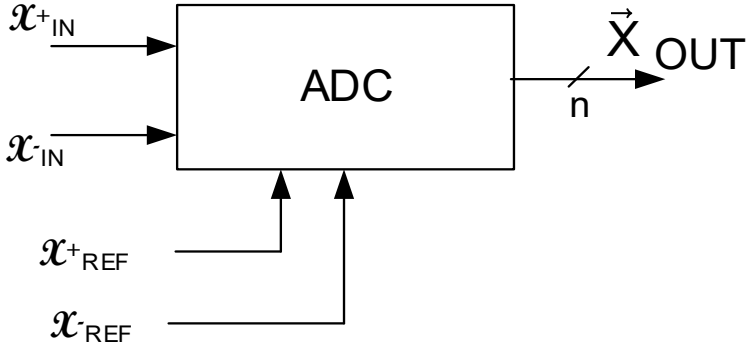


Input range is X_{REF}

Basic structure with differential inputs/references:



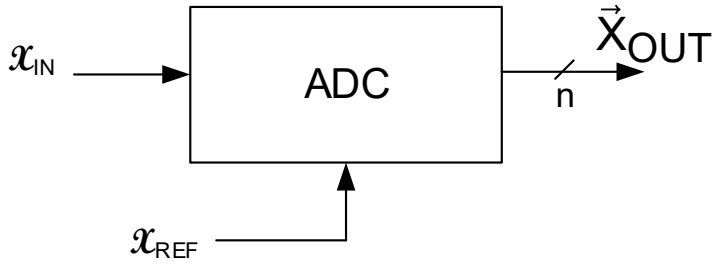
Input range is $X^+_{REF} - X^-_{REF}$

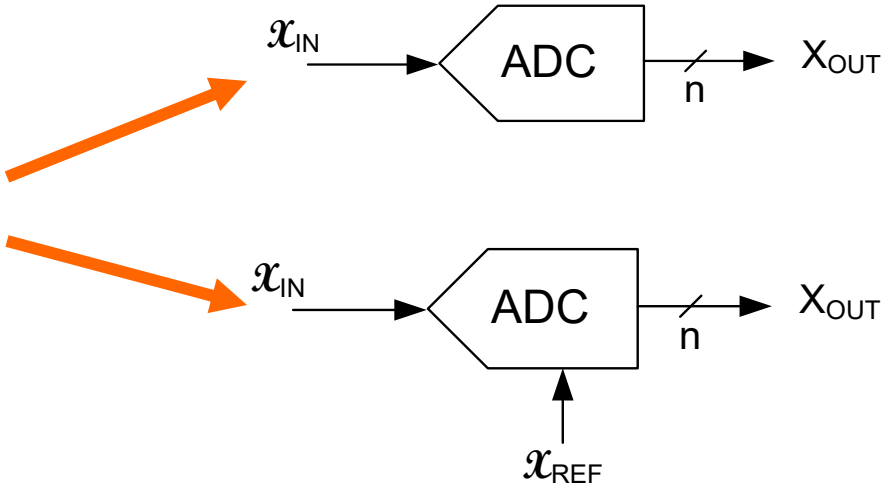


Input range is $2(X^+_{REF} - X^-_{REF})$

A/D Converters

Notation:





A/D Converters

$$\vec{X}_{OUT} = <d_{n-1}, d_{n-2}, \ldots d_0>$$

d_0 is the Least Significant Bit (LSB)

d_{n-1} is the Most Significant Bit (MSB)

Number of ideal ADC outputs: $N=2^n$

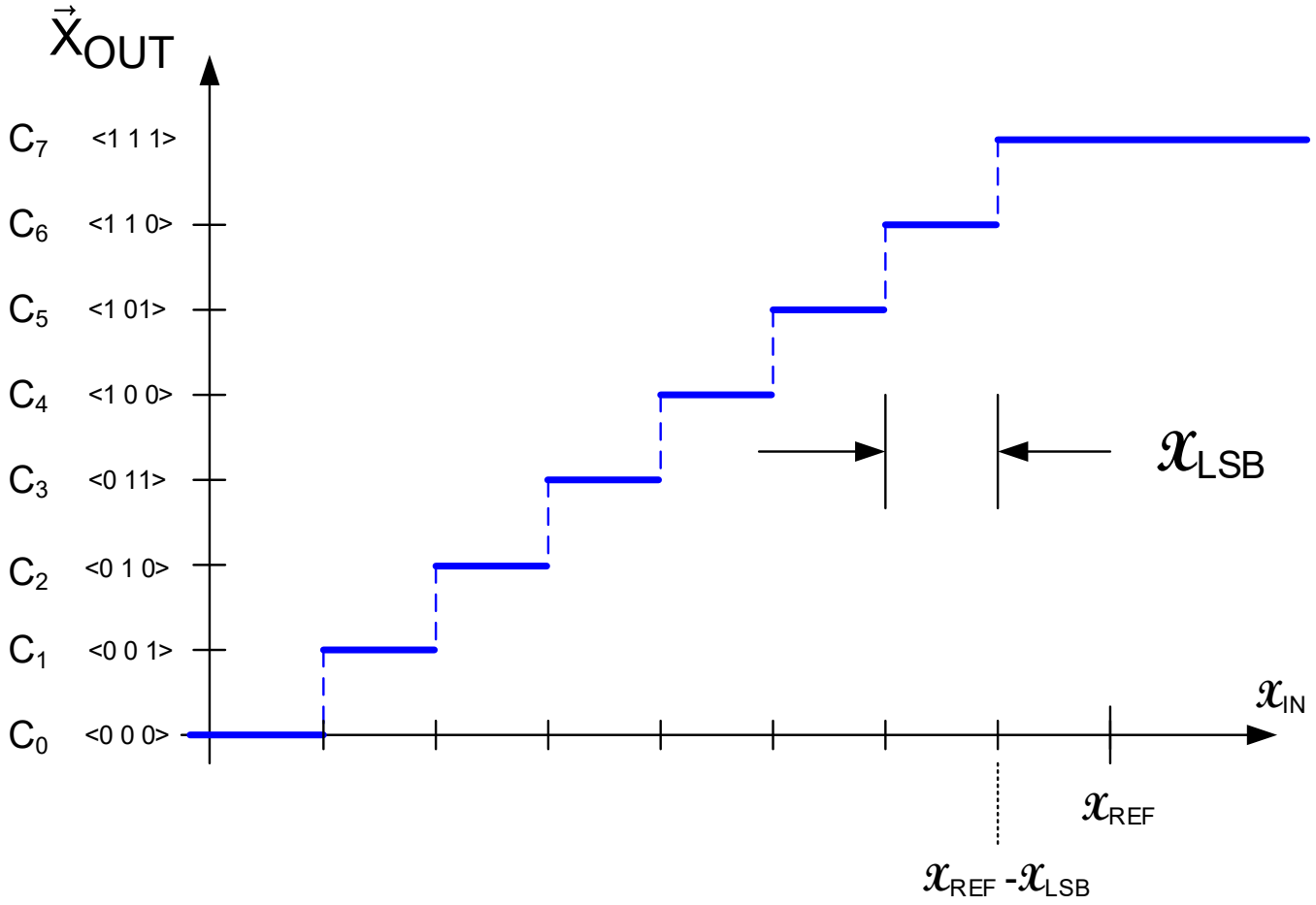
Note: some authors use different index notation

An Ideal ADC is characterized at low frequencies by its static performance

A/D Converters

An Ideal ADC transfer characteristic (3-bits)

$$\vec{X}_{OUT} = <d_{n-1}, d_{n-2}, \ldots d_0>$$



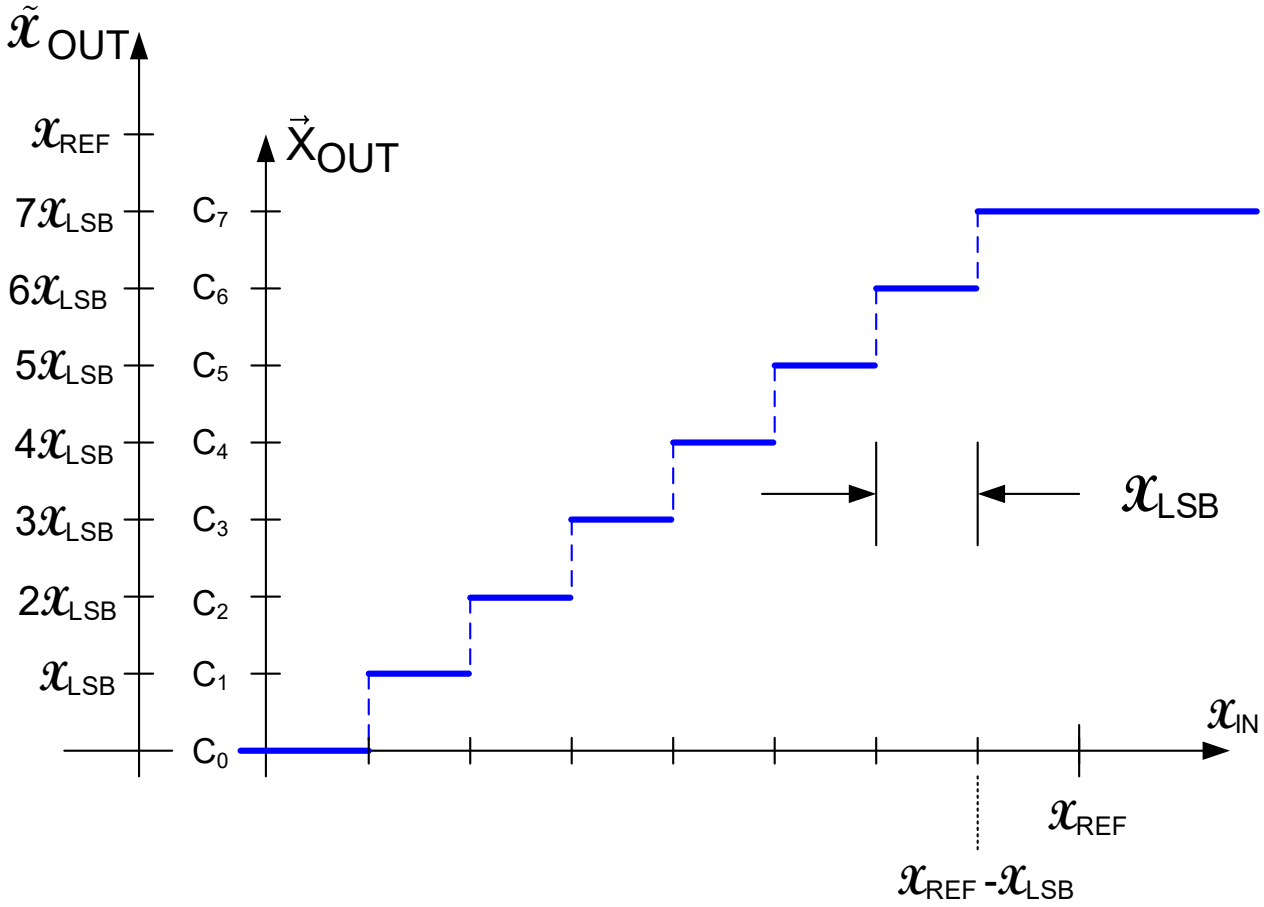
$$x_{LSB} = \frac{x_{REF}}{2^n}$$

A/D Converters

An Ideal ADC transfer characteristic (3-bits)

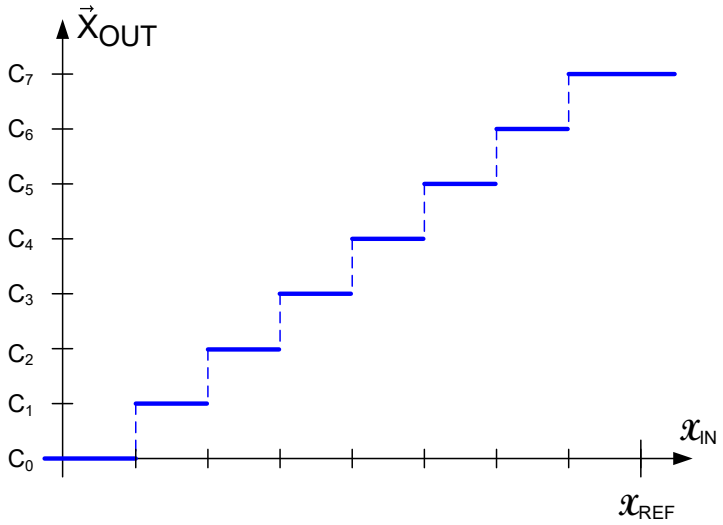
$$\vec{X}_{OUT} = \langle d_{n-1}, d_{n-2}, \ldots d_0 \rangle$$

$$x_{LSB} = \frac{x_{REF}}{2^n}$$



The second vertical axis, labeled $\tilde{x}_{OUT}$,is the interpreted value of $\vec{X}_{OUT}$

A/D Converters



For this ideal ADC

$$x_{REF}\left(\frac{d_{n-1}}{2}+\frac{d_{n-2}}{4}+\frac{d_{n-3}}{8}+\ldots+\frac{d_1}{2^{n-1}}+\frac{d_0}{2^n}\right)=x_{IN}+\varepsilon$$

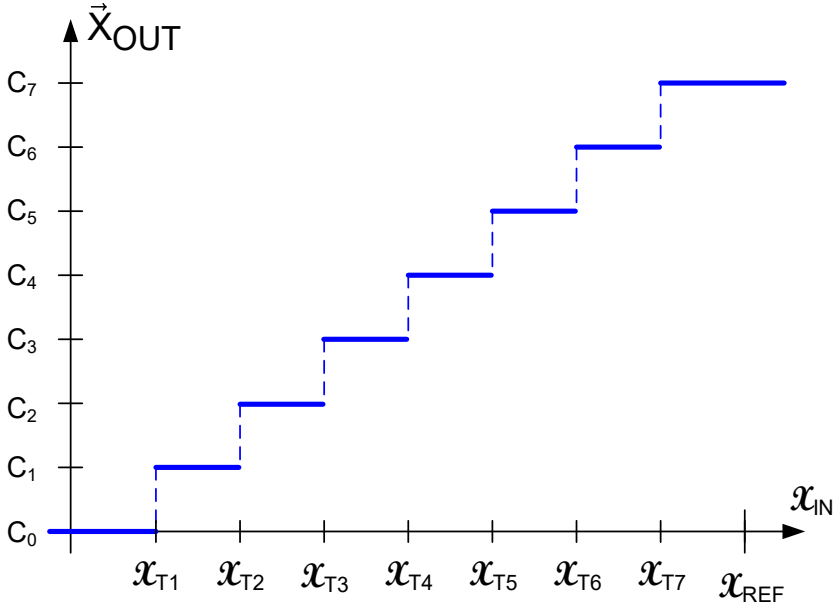
where ε is small (typically less than 1LSB)

$$x_{REF}\sum_{j=1}^{n}\frac{d_{n-j}}{2^j}=x_{IN}+\varepsilon$$

- Number of bins gets very large for n large
- Spacing between break points is $x_{REF}/2^n$ and gets very small for n large

ε is the **quantization error** and is inherent in any ADC

A/D Converters



Transition Points

- Actual values of x_{IN} where transitions occur are termed transition points or break points
- For an ideal n-bit ADC, there are 2^n-1 transition points
- Ideally the transition points are all separated by 1 LSB -- $X_{LSB}=X_{REF}/2^n$
- Ideally the transition points are uniformly spaced
- In an actual ADC, the transition points will deviate a little from their ideal location

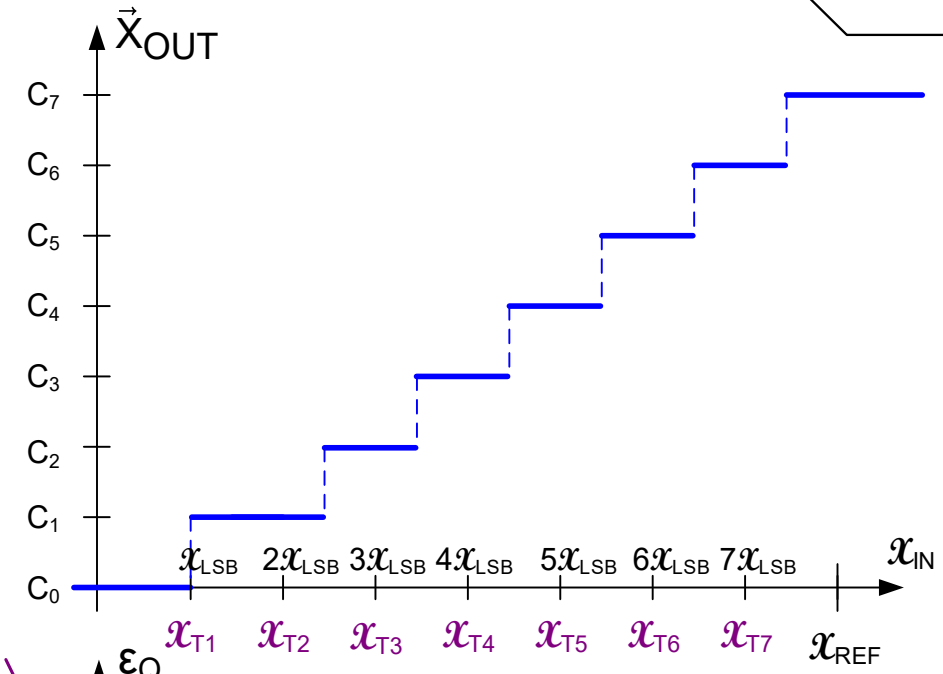
Labeling Convention:

We will define the transition point X_{Tk} to be the break point where the transition in the code output to code C_k occurs. This seemingly obvious ordering of break points becomes ambiguous, though, when more than one break points cause a transition to code C_k which can occur in some nonideal ADCs

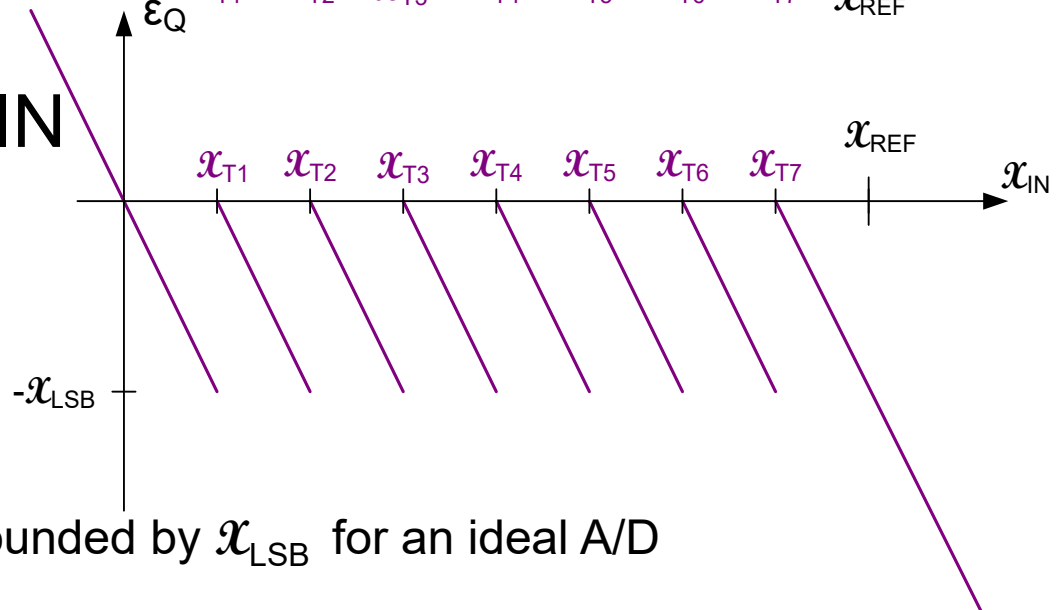
A/D Converters

Quantization Errors

$x_{T1}=x_{LSB}$



$$\varepsilon_Q = \tilde{x}_{OUT} - x_{IN}$$



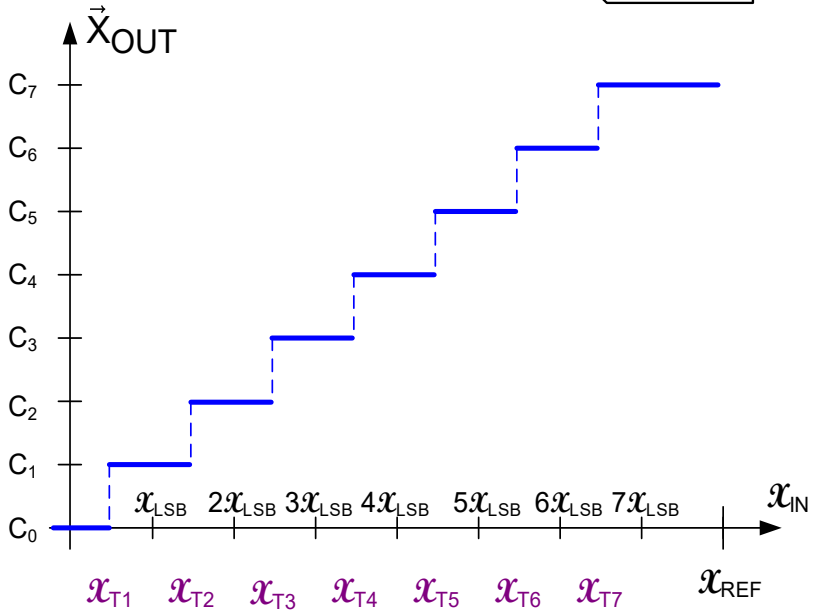
Magnitude of ε_Q bounded by x_{LSB} for an ideal A/D

A/D Converters

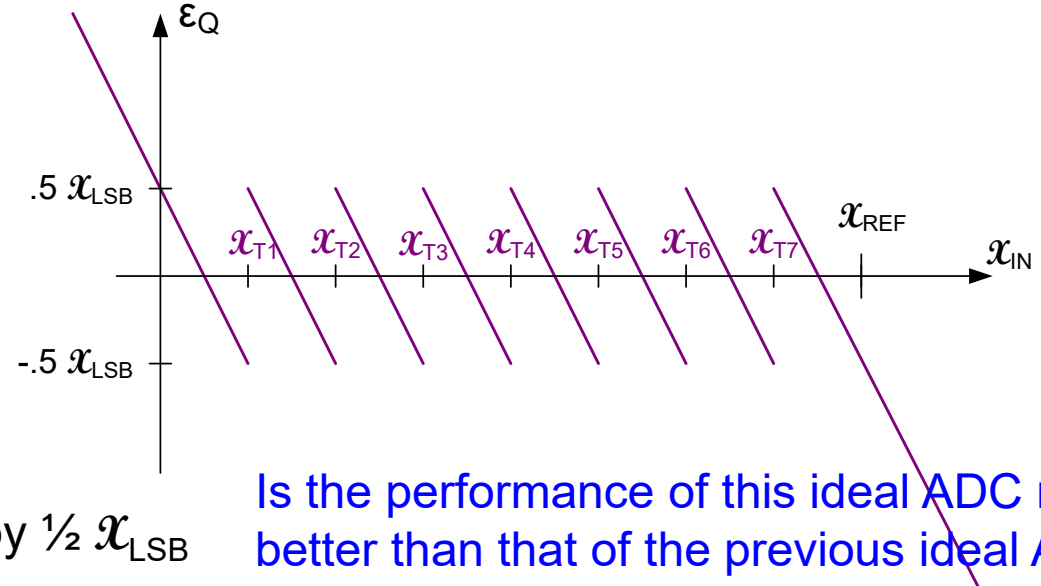
Quantization Errors

Another Ideal ADC

$x_{T1}=x_{LSB}/2$



$$\varepsilon_Q = \tilde{x}_{OUT} - x_{IN}$$



Magnitude of ε_Q bounded by ½ x_{LSB}

Is the performance of this ideal ADC really better than that of the previous ideal ADC?

Data Converter Architectures

- Large number of different circuits have been proposed for building data converters
- Often a dramatic difference in performance from one structure to another
- Performance of almost all structures are identical if ideal components are used
- Much of data converter design involves identifying the problems associated with a given structure and figuring out ways to reduce the effects of these problems
- Critical that all problems that are significant be identified and solved
- Many of the problems are statistical in nature and implications of not solving problems are in a yield loss that may be dramatic

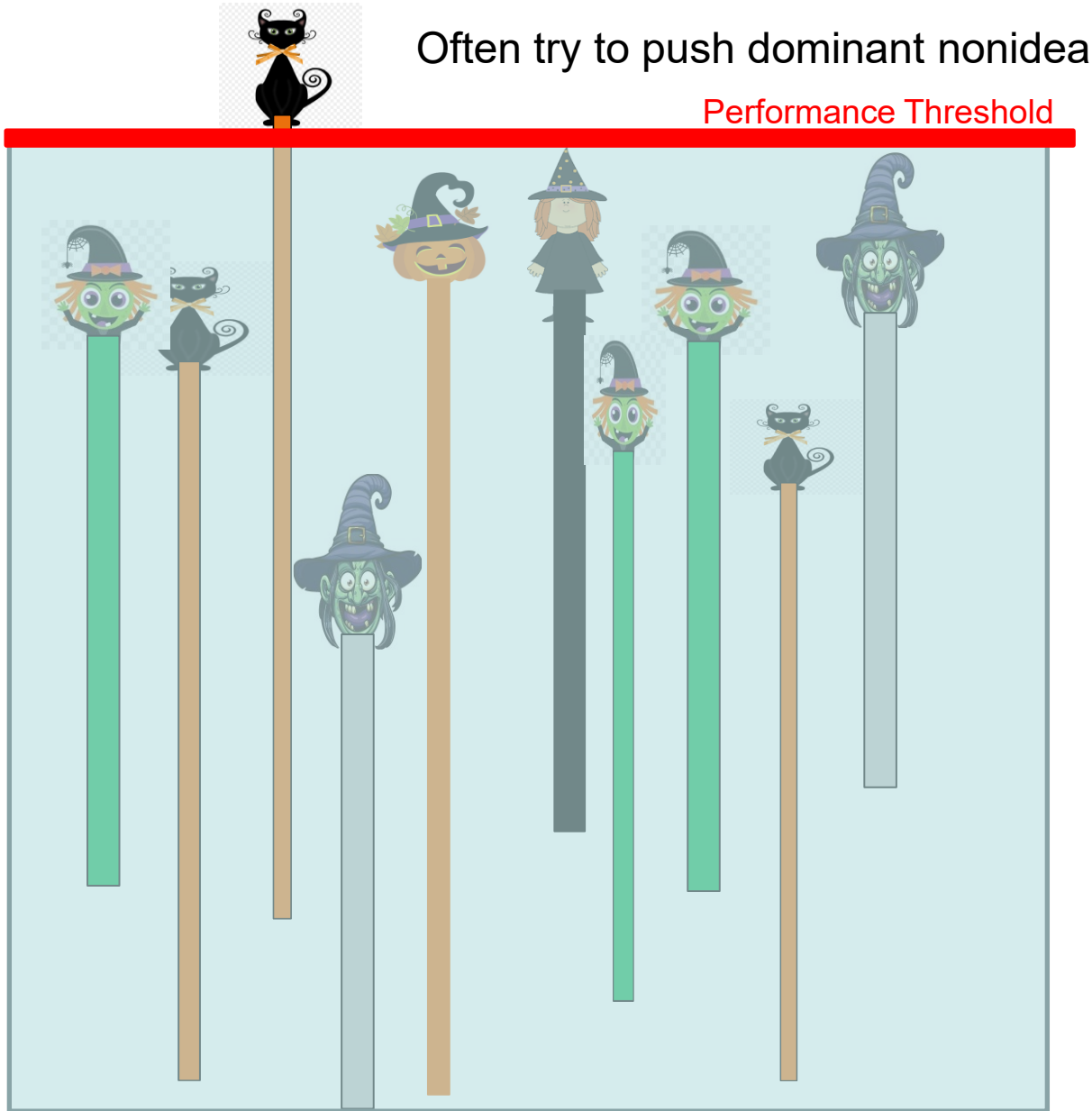
Data Converter Design Approach

Ideally all performance limitations below performance threshold

Data Converter Design Approach

Often one or two nonideal effects above performance threshold

Often try to push dominant nonideal effect down



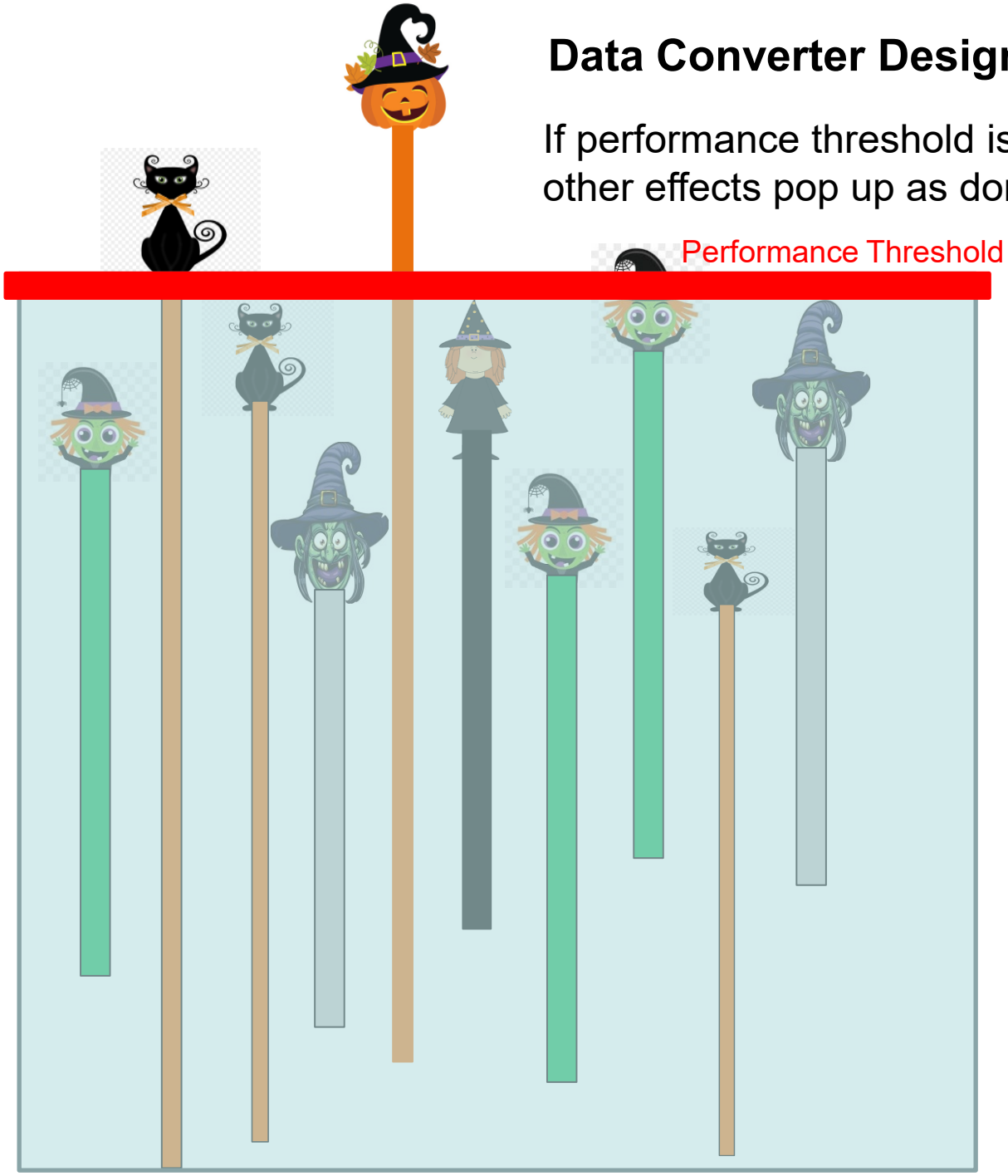
Data Converter Design Approach

Often one or two nonideal effects above performance threshold

Often try to push dominant nonideal effect down

Data Converter Design Approach

If performance threshold is made “higher”, other effects pop up as dominant

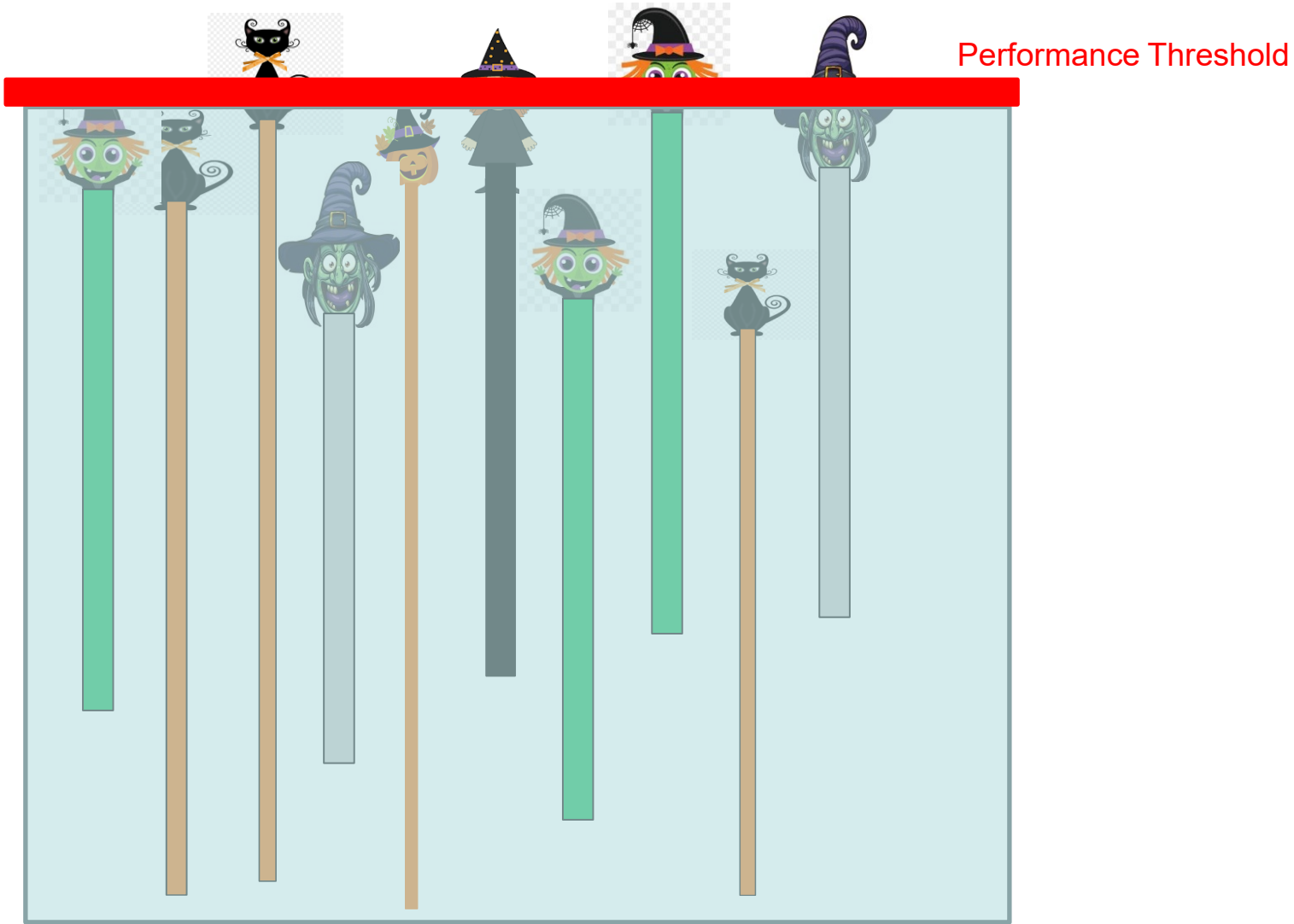


Data Converter Design Approach

Push them down too

Data Converter Design Approach

Ultimately enhancing performance threshold makes it more difficult to further improve performance



Data Converter Architectures

Strategy for discussing data converters

- Briefly look at some different data converter architectures
- Detailed discussion of performance parameters for data converters
- More detailed discussion of data converter architectures

Data Converter Architectures

Nyquist Rate

Flash
Charge Redistribution
Pipeline
Two-step and Multi-Step
Interpolating
Algorithmic/Cyclic
Successive Approximation (Register) SAR
Single Slope / Dual Slope
Subranging
Folded
Interleaved

Current Steering
R-string
Charge Redistribution
Algorithmic
R-2R (ladder)
Pipelined
Subranging

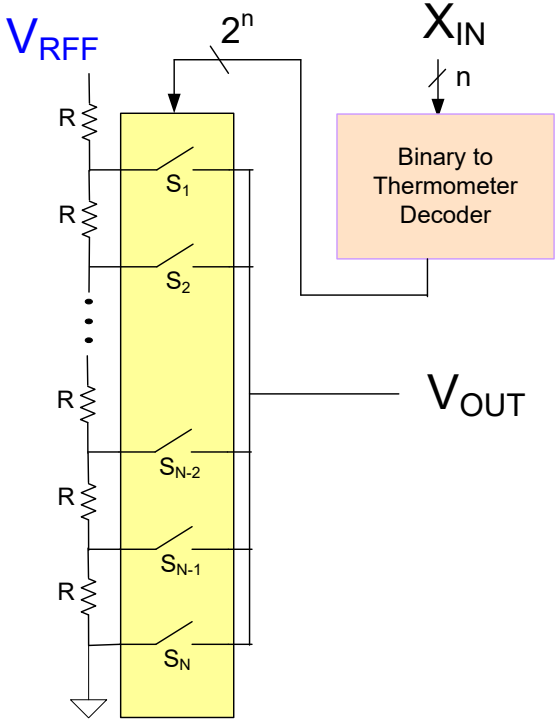
Over-Sampled (Delta-Sigma)

Discrete-time
First-order/Higher Order
Continuous-time

Discrete-time
First-order/Higher Order
Continuous-time

Data Converter Architectures

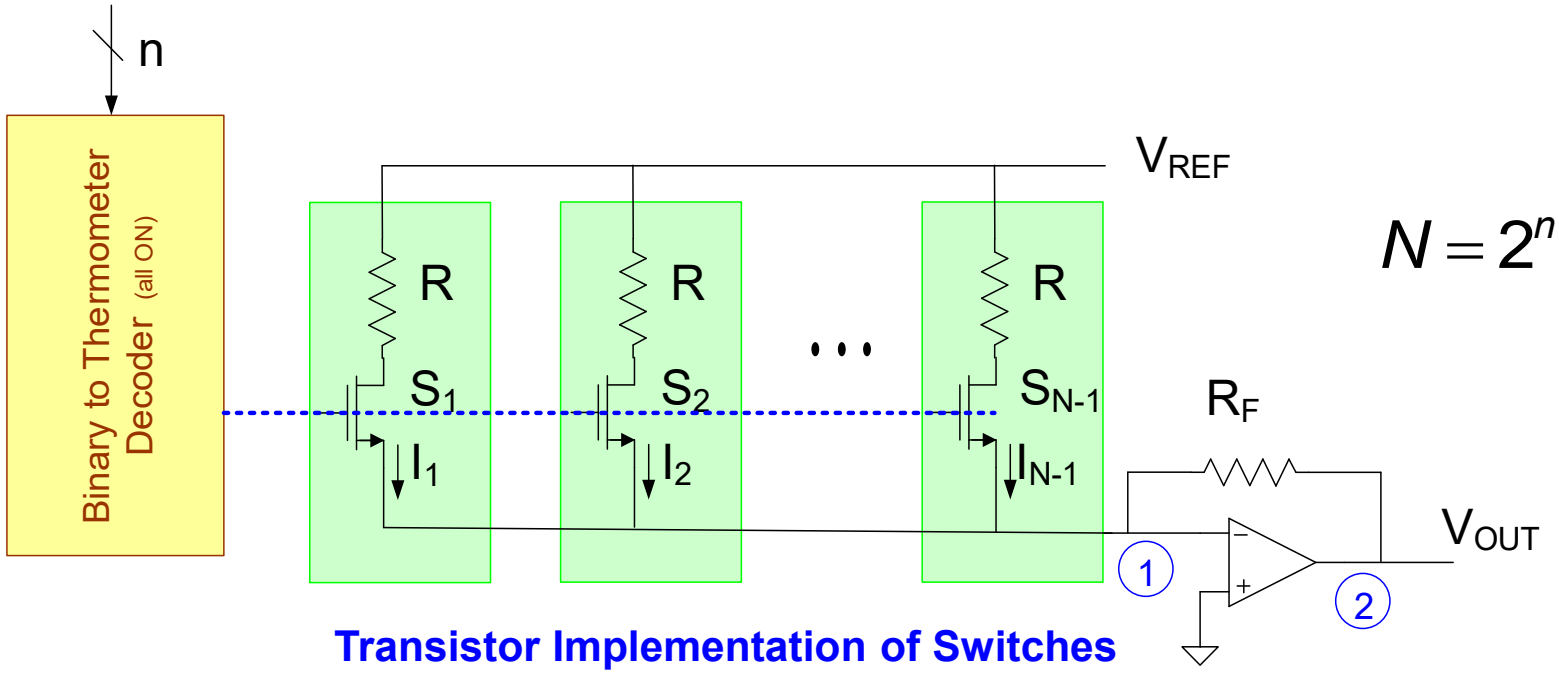
R-String DAC



Basic R-String DAC including Logic to Control Switches

Data Converter Architectures

Current Steering DAC

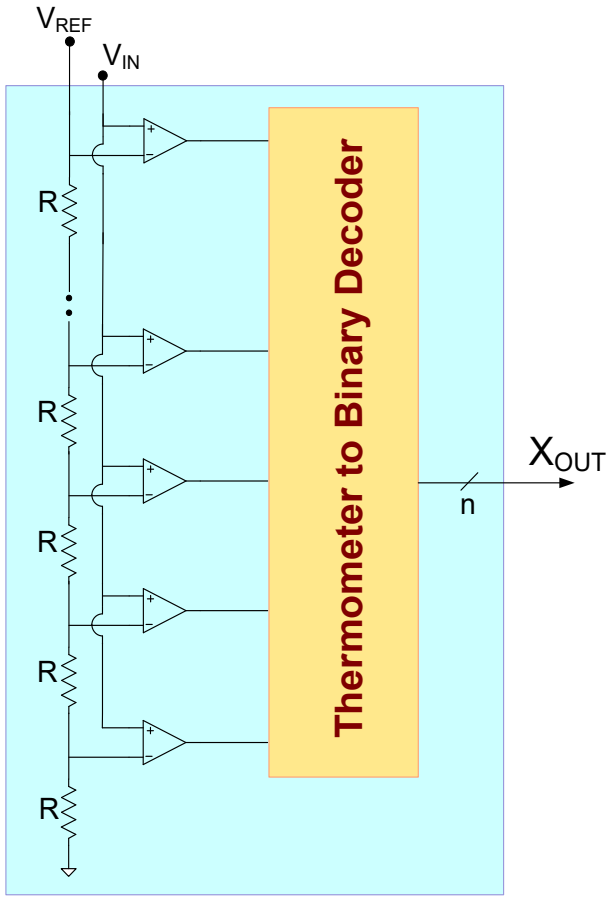


Transistor Implementation of Switches

Assume k switches are on 0<k<N-1 as determined by digital input code

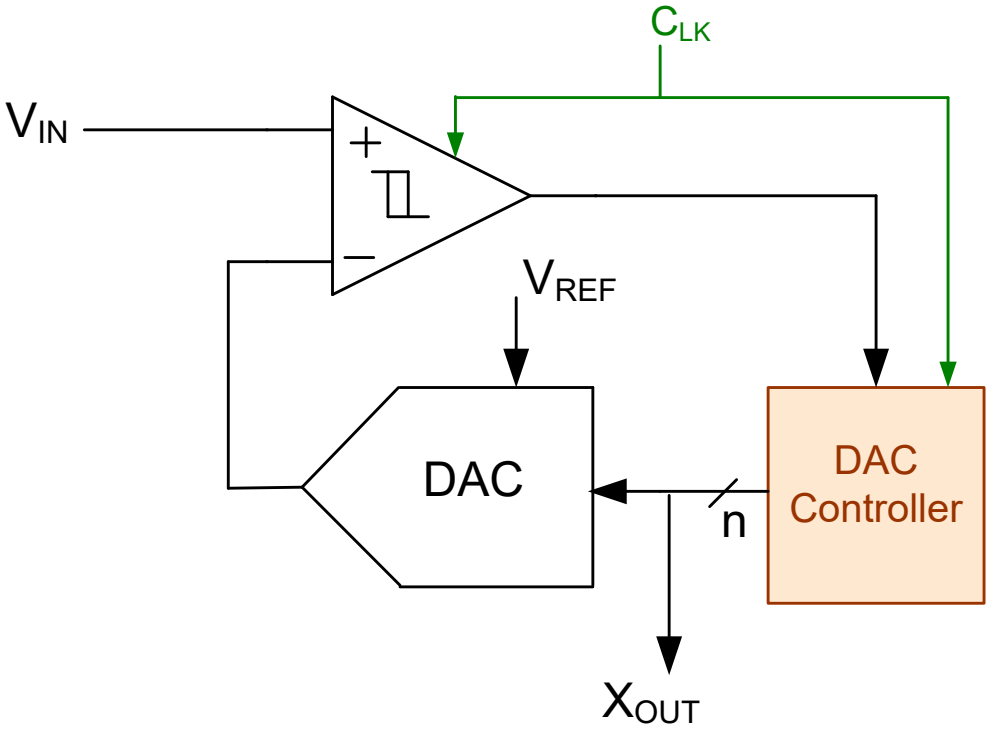
Data Converter Architectures

Flash

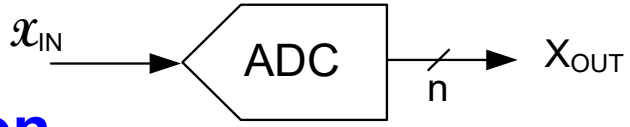


Data Converter Architectures

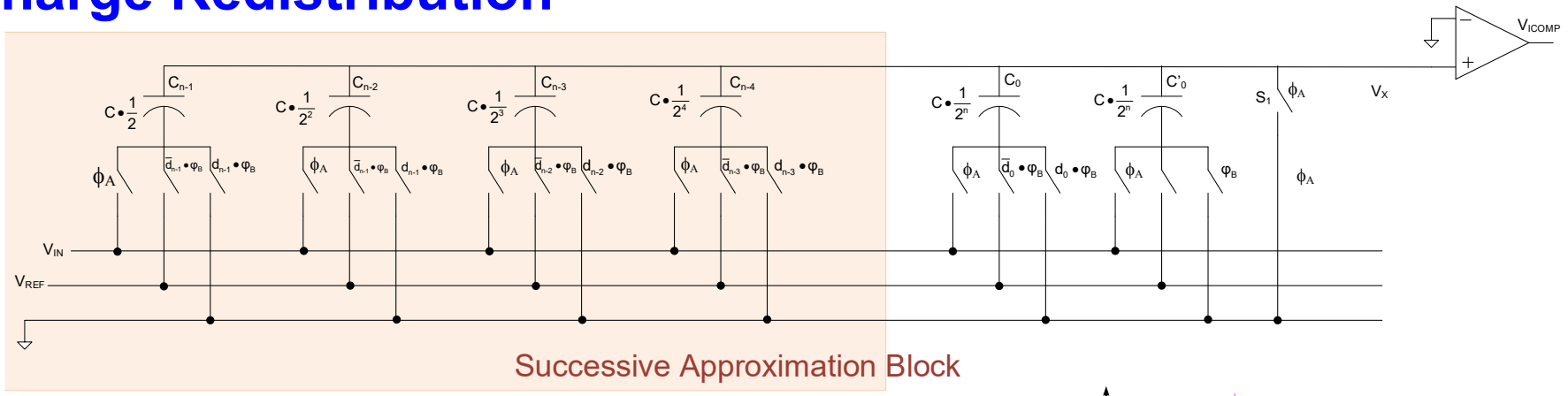
Successive Approximation Register (SAR)



Data Converter Architectures



Charge Redistribution



Redistribute charge with switches to drive Vx to 0

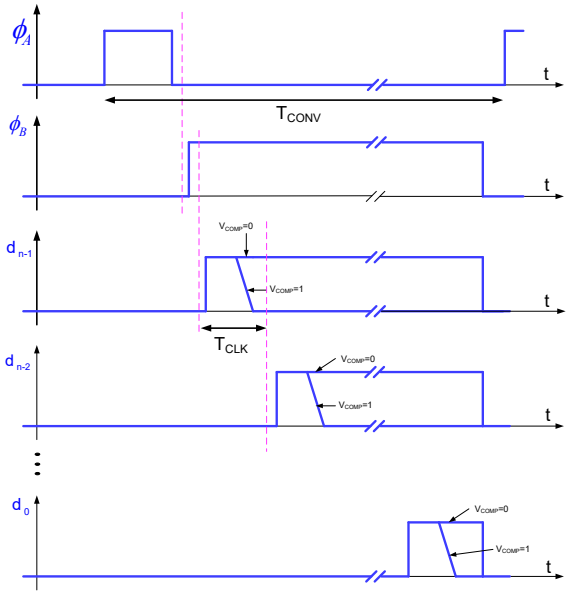
$$Q_{SAM} = V_{IN}\left(\sum_{i=0}^{n-1} C_i + \left[C_0^{'}\right]\right) = V_{IN}\left(\sum_{i=0}^{n-1} \frac{C}{2^{n-i}} + \left[\frac{C}{2^n}\right]\right) = V_{IN}C$$

$$Q_{REDIS} = V_{REF}\sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}}$$

$$Q_{SAM} = Q_{REDIS}$$

$$V_{REF}\sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{IN}C$$

$$V_{IN} = V_{REF}\sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$



Stay Safe and Stay Healthy !

End of Lecture 24